REMARKS

Claims 5, 8, 10, 11, 33, 37, 47, 48, 53, 54, 70-72, 74-78, 80 and 81 are pending in the application, with claims 5, 8, 70 and 76 being independent. Claims 1-4, 6, 7, 9, 12-32, 34-36, 38-46, 49-52, 55-69, 73 and 79 have been canceled.

Initially, applicant submits that the double patenting rejections are moot in view of the cancellation of claim 1 and its dependent claims.

Claim 5 has been amended in response to the rejection under section 112, second paragraph. This amendment is believed to address the rejection in that claim 5 now more clearly recites that the digital signals corresponding to m frames are stored in the n x m memory circuits.

Independent claims 5, 8, 70 and 76, as well as many of their dependent claims, have been rejected as being unpatentable over Natano (JP 410253941) in view of Yokoyama (US2001/005193). Claims 5, 8, 70 and 76 have been amended. In particular, each of the independent claims has been amended to recite that each of the pixels has n gate signal lines and n TFTs having gate electrodes, with each of the gate electrodes being connected to a corresponding one of the n gate signal lines. This recitation finds support in the application at, for example, Fig. 1, which shows gate signal lines 102-104 and TFTs 108-110 having gate electrodes, with each of the gate electrodes being connected to a corresponding one of the gate signal lines.

Applicant requests reconsideration and withdrawal of this rejection because neither Natano, Yokoyama, nor any proper combination of the two describes or suggests a pixel in which gate electrodes of n TFTs are corrected to corresponding ones of n gate signal lines.

As noted by the Examiner, Natano does not describe or suggest having multiple gate electrodes of TFTs of a pixel connected to corresponding ones of multiple gate signal lines. Instead, the pixel circuit (14) of Natano includes only a single gate line (11).

While the Examiner appears to rely on Yokoyama as describing a connection such as is recited in the claims, Yokoyama also describes a pixel (200) having only a single gate line (51).

Accordingly, since both Natano and Yokoyama fail to describe or suggest a pixel having multiple gate signal lines and multiple TFTs, with the gate electrode of each TFT being

connected to a corresponding one of the gate signal lines, no proper combination of Natano and Yokoyama can describe or suggest this arrangement. Accordingly, the rejection should be withdrawn.

Dependent claims 10, 11, 77 and 78 have been rejected as being unpatentable over Natano in view of Yokoyama and further in view of Kinoshita. Applicant requests reconsideration and withdrawal of this rejection because Kinoshita does not remedy the failure of Natano and Yokoyama to describe or suggest the subject matter of the independent claims.

Applicant submits that all claims are in condition for allowance.

Enclosed is a $290 check for the Information Disclosure Statement fee ($180) and the Petition for Extension of Time fee ($110). Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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